REMARKS

Claims 1-18 are pending in this application. Claims 1, 7, 13-15 and 18 have been amended by the present Amendment. Amended claims 1, 7, 13-15 and 18 do not introduce any new subject matter.

REJECTION UNDER 35 U.SC. § 112

Reconsideration is respectfully requested of the rejection of claims 1-18 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner maintains that "capable of merely suggests or makes optional, but does not require steps to be performed, or does not limit a claim to a particular structure."

Applicants have amended claims 1, 7, 13-15 and 18 to delete "capable of".

Accordingly, Applicants respectfully request that the Examiner withdraw the rejection of claims 1-18 under 35 U.S.C. § 112.

REJECTION UNDER 35 U.SC. § 103

Reconsideration respectfully requested of the rejection of claims 1-18 under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art (APA) in view of U.S. Patent Application Pub. No. 2003/0177293 ("Bilak").

The Cited References Do Not Disclose The Claimed Buffer Memory

Claims 1, 7, 13 and 18 recite a buffer memory having transmitting and receiving areas performing flexible memory allocation. For example, the buffer memory 210 includes transmitting and receiving areas having flexible memory allocation according to transmitted and received data flow, thereby reducing data overflow or underflow during data communication. See, e.g., Applicants' disclosure, page 2, lines 26-28; page 7.

lines 1-4; and Fig. 2.

The Examiner maintains that APA discloses a buffer memory in the form of transmitting memory 110 and receiving memory 130. <u>See</u> December 1, 2006 Office Action at 3

However, in contrast to the claimed embodiments, the transmitting and receiving memories 110, 130 are two separate memories, which are more likely to cause data overflow or underflow. The embodiments of claims 1, 7, 13 and 18 recite the buffer memory having transmitting and receiving areas, which are flexibly allocated.

In addition, unlike the claimed embodiments, Bilak also shows two separate buffer spaces 450 and 460. See Bilak, Fig. 1.

Therefore, unlike APA and Bilak, the embodiments of claims 1, 7, 13 and 18 recite the common buffer memory having the transmitting and receiving areas, not separate memories, so as to reduce data overflow or underflow.

For at least this reason, Applicants respectfully submit that claims 1, 7, 13 and 18 are patentable over APA in view of Bilak.

The Cited References Do Not Disclose Generating And Outputting Threshold Control Signals (THS) As Claimed

Claims 1, 7, 13 and 18 recite generating and outputting threshold control signals for increasing memory allocation of the transmitting area when a transmission execution signal becomes active and for increasing memory allocation of the receiving area when a reception execution signal becomes active.

For example, activity of the transmission execution signal (TXEX) triggers the threshold control signal (THS) to be transmitted to the transmitting controller 230, resulting in an instruction to increase memory allocation of a transmitting area of a

buffer memory 210. In addition, activity of the reception execution signal (RXEX) triggers the threshold control signal (THS) to be transmitted to the receiving controller 240, resulting in an instruction to increase memory allocation of a receiving area of the buffer memory 210. See, e.g., Applicants' disclosure, Fig. 2; page 7, line 27 – page 8, line 31; page 9, lines 20-23; and page 10, lines 1-4.

The Examiner maintains that Bilak discloses a flow control unit in the form of processing thread 120 for generating and outputting threshold control signals, which Examiner analogizes to R RDY signals. See December 1, 2006 Office Action at 4.

However, in contrast to the claimed embodiments, the R_RDY is not a threshold control signal. In other words, the R_RDY is not used for controlling memory allocation. In contrast, requests for data transmission are sent through one or more R_RDY's. However, such requests are not controlling memory allocation.

Indeed, there is no control signal in Bilak for increasing memory allocation. Unlike the claimed embodiments, Bilak only queries whether a buffer has enough space for a frame. See Bilak, Figs. 3 and 5, (elements 350 and 640). If it is determined that the buffer has enough space, then the data is stored in that buffer. If there is insufficient space in the dedicated buffer and there is sufficient space in the other buffer to accommodate the frame, data is stored in the other buffer. See Bilak, ¶¶ 0033 and 0037. However, unlike the claimed embodiments, there is no judgment being made of whether a signal (i.e., TXEX, RXEX) is an active state in order to generate a threshold control signal. Indeed, Bilak only estimates whether an inbound buffer has enough space.

Therefore, unlike APA and Bilak, the embodiments of claims 1, 7, 13 and 18

recite generating and outputting threshold control signals for increasing memory allocation when a transmission or reception execution signal becomes active, not merely querying whether a buffer has sufficient space for data.

For at least this reason, Applicants respectfully submit that claims 1, 7, 13 and 18 are patentable over APA in view of Bilak.

The Cited References Do Not Disclose Generating TXEX and RXEX Based On Receipt Of Data

Claims 1 and 7 recite that the transmission execution signal becomes active upon receipt of data from the system bus, and that the reception execution signal becomes active upon receipt of data from the lower layer.

For example, the receipt of data SYSTD by the transmitting controller 230 from the system bus triggers activity of the transmission execution signal (TXEX), which is output to the flow controller 220. The receipt of data PHYRD by the receiving controller 240 from the lower layer triggers activity of the reception execution signal (RXEX), which is output to the flow controller 220. See, e.g., Applicants' disclosure, Fig. 2; page 7, line 27 – page 8, line 31; page 9, lines 20-23; and page 10, lines 1-4.

As recited in the claimed embodiments, the transmission and reception execution signals are generated according to received data.

In contrast to the claimed embodiments, Bilak does not generate or output any signals according to received data. Bilak discloses only querying whether a buffer has enough space for a frame, and does not cause transmission or reception execution signals to become active upon receipt of data. <u>See</u> Bilak, Figs. 3 and 5, (elements 350 and 640).

As such, for at least this reason, Applicants respectfully submit that claims 1 and

7 are patentable over the APA in view of Bilak.

Conclusion

As such, for at least the above reasons, Applicants respectfully submit that claims 1, 7, 13 and 18 are patentable over the APA in view of Bilak.

For at least the reason that claims 2-6 depend from claim 1, claims 8-12 depend from claim 7, and claims 14-17 depend from claim 13, claims 2-6, 8-12, and 14-17 are also submitted to be patentable over the cited references.

Therefore, Applicants respectfully request that the Examiner withdraw the rejection of claims 1-18 under 35 U.S.C. § 103(a).

DEPENDENT CLAIMS

Applicants have not independently addressed the rejections of all the dependent claims because Applicants submit that, in view of the amendments to the claims presented herein and, for at least similar reasons as why the independent claims from which the dependent claims depend are believed allowable as discussed, supra, the dependent claims are also allowable. Applicants however, reserve the right to address any individual rejections of the dependent claims should such be necessary or appropriate.

An early and favorable reconsideration is earnestly solicited. If the Examiner has any further questions or comments, the Examiner may telephone Applicants' Attorney to reach a prompt disposition of this application.

Respectfully submitted,

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